International Journal of Advance Research and Innovation
Vol. 8(2), Apr-Jun 2019, pp. 81-86
Doi: 10.51976/iiari.822014

Article Info

Received: 17 Jan 2020 | Revised Submission: 20 May 2020 | Accepted: 28 May 2020 | Available Online: 15 Jun 2020

VLSI Architecture for Zero Frequency Filter

Bosebabu P., Bhargavi A.**, Vijayalakshmi P.* and Surabhi Jyostna Roja R.**

ABSTRACT

Now a days everyone is using mobile phones. Mobile phones play an important role in communication. While using mobile phones, people face the problem of noise signals. These noise signals are affecting the quality of speech signals. These noise signals maybe produced from the materials or sources such as echoes, crowded places, etc. For example, when we speak over the mobile phone or in any crowded place, the external noise adds up like the noise of the subway, train, car, etc. In real time to remove external noise is a very crucial task. A lot of research has been done in cancelling the background noise reduction. Acoustic noise is a type of noise which can produce unwanted sound and it can be reduced by selecting a higher switching frequency (at the cost of higher inverter losses). So a new technique was introduced called passive noise cancellation that supresses higher frequency acoustic noise. In order to supress the lower frequency, the passive techniques require materials that is too bulky and heavy. For these materials, an alternative method is required known as active noise cancellation. This technique does not come without its change as it is used to actively cancel the noise of the world around you to make your audio come clearer. Active noise cancellation separates noise signal and the speech signal is chosen. In order to use active noise cancellation, we use zero frequency filter technique for the cancellation of noisy speech signals. It is used for detecting the regions of glottal activity and in estimating the strength of excitation n each glottal cycle. The main advantage of active noise cancellation is to cancel the random sounds due to repetition in the waveform. ANC is used in the reduction by using a power source. It is best suited for low frequencies. VLSI architecture for zero frequency filter can be used as a voice processor in mobile applications. The existing system has produced a time delay of 220ps. In this paper, we are reducing the time delay into 120ps by using tanner tool software.

Keywords: *Active noise cancellation; Zero frequency filtering; Acoustic noise.*

1.0 Introduction

Noise is an unwanted signal. In communication systems, noise is an error or undesired random disturbance of a useful information signal. Noise is the summation of unwanted energy from natural and sometimes man-made sources. There are several ways to classify noise but conveniently noise is classified as external noise and internal noise. External noise is defined as the noise that is generated externally due to communication. These are classified as atmospheric noises, industrial noises and terrestrial noises. Internal noise is generated within the communication system or in the receiver. These can be classified as low frequency, high frequency and thermal noises. Zero frequency filter is the signal that has zero frequency. DC signal is filtered by using zero frequency filter which is used in active noise cancellation method. Here we are using adders to decrease DC noises. Some of the DC noises are thermal, shot, flicker, burst and transit time noises.

Active noise cancellation or active noise control or active noise reduction is a method for reducing the unwanted sound specifically designed to cancel the first. It works by using microphones to pick up low frequency noise and neutralise it before it reaches the ear. In this project we have taken active noise cancellation method as it can reduce noise that has low frequencies as well as high frequencies, whereas passive noise cancellation can reduce only high frequencies.

** Department of Electronics and Communication Engineering, BITS, Vizag, Andhra Pradesh, India.*
***Corresponding author; Department of Electronics and Communication Engineering, BITS, Vizag, Andhra Pradesh, India. (E-mail: arige.bhargavi21@gmail.com)*

The main aim of active noise cancellation is to generate an anti- noise signal from ambient noise to reduce the noise level of the original signal.

2.0 Literature Survey

Speech is the output of time varying local tract system excited by a time varying excitation. In resulting speech signal, the information of speech production system is embedded as relations in the sequence of values of signal at different instants of sampling signal. The main objective of speech signal processing is to extract information of time varying characteristics of speech production system [1].The information is represented in the form of parameters or features derived from the signal. Clock tree synthesis is a fundamental step in physical design. If targeting global zero skew it would cost in area or power and limit achievable operating frequency. Data path optimization is not sufficient to handle timing violations [2].

A very straight forward approach in noise cancelling is the use of LMS algorithm [3] which was developed by Windrow and Hoff. This algorithm uses a gradient descent method that finds a minimum, if it exists by taking steps in the direction negative of gradient and it does by adjusting filter coefficients in order to minimize error. The speech signals collected simultaneously using pair of spatially separated microphones in real room environment. The spatial separation results in fixed time delay of arrival of speech signals from given speaker at a pair of microphones [4]. The time delays are estimated for exploiting impulse like characteristic of excitation during speech production. Zero frequency filtering is a technique used in the characterization and analysis of glottal activity from speech signals. IIR filters followed by two successive finite impulse response filters [5]. The integrated variation analysis technique is considered for the effects of both systematic and random variation in interconnect and devices to get better perspective on the impact of variation [6]. By exploiting useful clock skew, it can help reduce timing violations rapidly. Multi-corner multimode design flow can analyse over MCMM scenarios concurrently. It employs new analysis data model which advantages data duplication across various timing graphs. To solve this MCMM problem, chip level clock tree synthesis is used to reduce divergence between IPS for different corners. All papers [7-11] all are related to same topic of clock skew optimisation.

Engineering change order (ECO) is always used after detail routing in order fix violations of time by incremental adjustment [11].clock scheduling is a problem in several work studies in [12-14].But in all case the problem is clock optimisation period. Both this work is considering the delay but not the speeding up of the clock arrival. A novel clock tree re-synthesis methodology is presented to trickle all these issues. Instead of estimating clock schedule at the leap level registers, the author considered offsets in clock arrival at the clock tree driver pins of any designs which are already synthesized and routed clock tree.

In adaptive filters various algorithms are available such as LMS, NLMS for active noise cancellation [16-17]. Namely the glottal flow is the major source of excitation to convey the useful complementary information. Glottal flow is the air flow passing through the folds at the glottis. Hilbert envelop method, group delay method are used for extracting the glottal activity from speech signals in the papers such as [18-21].

Significant excitation of the vocal track system during production of speech is the Epoch the most challenging task is the extraction of epoch from speech signals.

3.0 Existing System

In this Zero frequency filtering technique is used to filter out the necessary instants of excitation those are not affected by time varying resonances from vocal track. Voiced and Non-Voiced detection involves identifying the region of speech if there is a significant glottal activity [23].The speech signal is the combination of both voiced and non-voiced or the background voice.

In this it target the zero skew which limits the achievable operating frequency to the maximum data path delay in the circuit. Useful clock skew means the clock is skewed intentionally then that is called as useful clock skew.

The timing slack is increased on the critical path, the timing can be met with impossible timing constraints, such as the input delay that is more than the time of a clock cycle. This can be done by skewing the receiving flip-flop as it does not create a

hold time problem. In this the technique used is the clock skew optimization based on the time.

In the figure 1, shows the Zero frequency filter blocks which are used to filter out all the non-voiced signals in the zeroth position of the signal. The differentiator is used to acts as the high pass filter and which supress the low frequency signals. The resonator used to select the single frequency and the detrendor block is used to select the particular trend in the signal which are higher highs and lower lows. The figure 2, shows that the delay for above fiter is approximately equal to the 200ps which is caused by using clock skew optimisation. For single flip-flop only it got such delay .The main target of this filter is decreases the dc signals in speech signals as well as decreases the time delay.

Figure 1:Delay Analysis

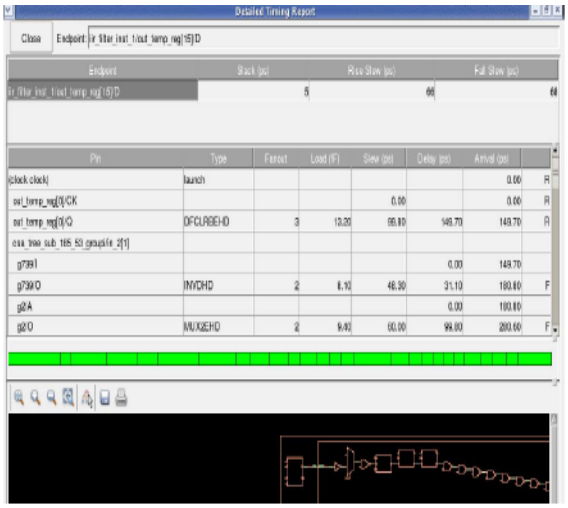
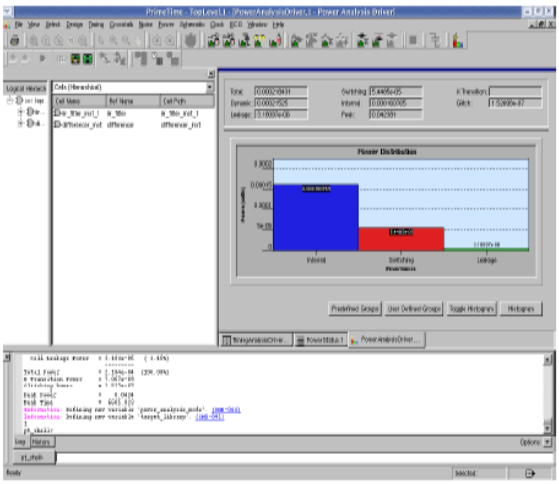


Figure 2: Power Analysis

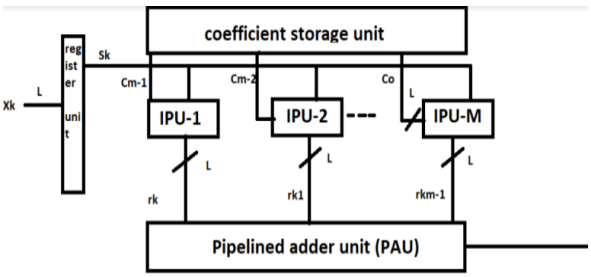


But in the case of existing system the filter designing is consentrated only on the decreasing of non-voiced signals it does not design for decreasing the delay and end the author concluded that the filter decreases the area about 15.87% and this fiter is implemented in 180nm technology using cadence RTL compiler and Encounter RTL-to-GDSII system with an operating frequency of 600MHz. In the Physical design process,The timing closure is achieved by useful clock skew optimization. The Fig2 shows the power analysis in the existing filter.

4.0 Proposing System

In the proposing system the filter is designed such that the both decreasing of delay and supreesing of dc signals in the speech signals can be done using the single filter only.

Figure 3: Block Diagram of Zero Frequency Filter



In this instead of using the flip-flop circuits, the adders are used by Active noise cancellation technique It leads to decrease the delay and it can also supress the non-voiced or back ground voice signal with minimum delay. The proposed system consists of four flip-flops are used in that the adder circuits are utilized to minimize the delay. Here the input signals are three those are speech signal, Noise signal and carry signal why because we are using the adders so the carry signal is need to give as input to the filter.

Here, when the three inputs are given then the outputs are two signals those are sum and carry, the carry from first flip-flop again give as the carry for the second flip-flop such that up to four flip-flops are connected. The main output is generated from the fourth flip-flop which is the sum. By comparing the input delay and the output sum delay is decreased. This filter is implemented in tanner tool. In this we can calculate the dc analysis, power analysis can be measured

Figure 4: Input and Output Components Used in the Filter

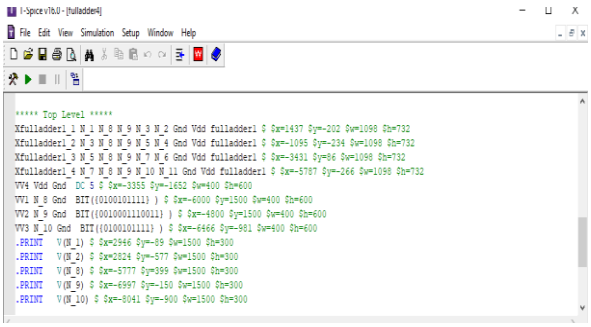
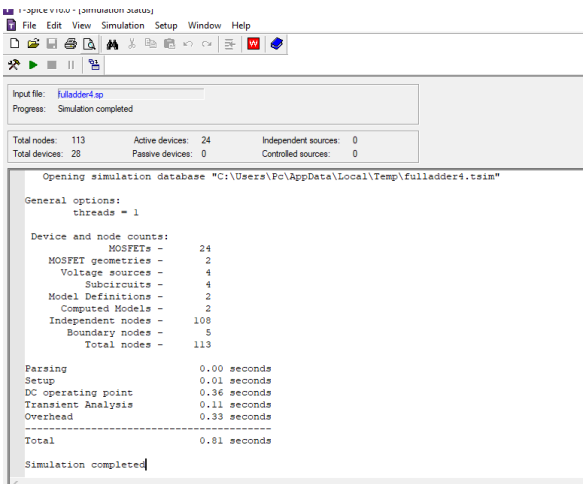


Figure 4, shows the details about the input and output components details these details are produced in the simulation time only.

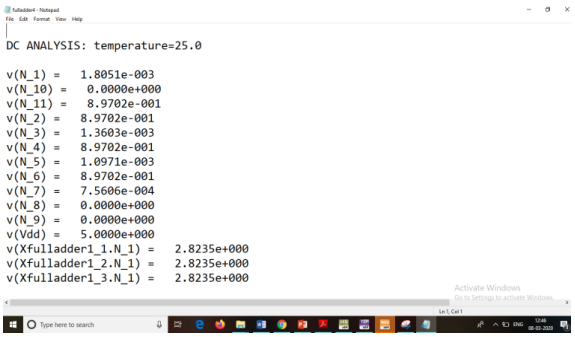
Figure 5: During Simulation Components Details



In all the components used in the circuit details can be obtained. And number components are used also obtained and delay results of every component in the circuit diagram

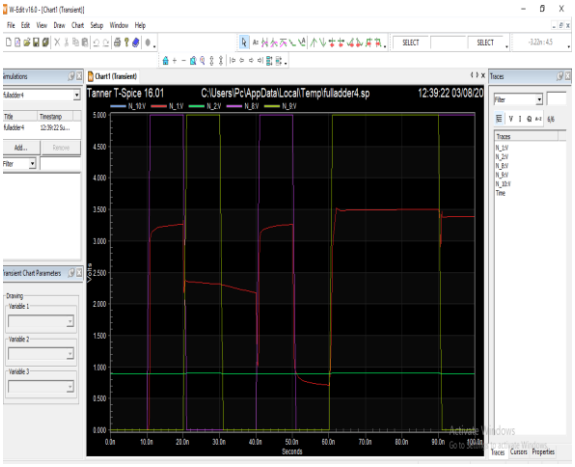
5.0 Results

Figure 6: Dc Analysis



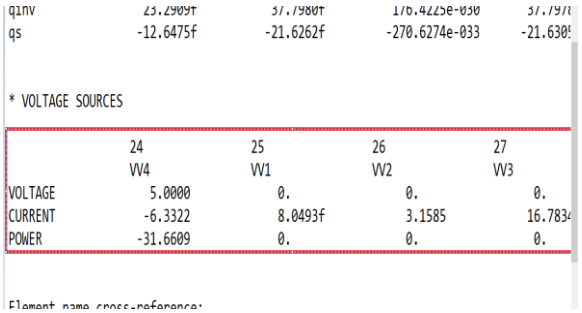
The figure 6, shows the results of dc analysis, it can shows the temperature of each component and whole circuit also. These all results are produced in another folder.

Figure 7: Output Waveforms



The output waveforms are generated with decreasing of delay with approximatly 125ps delay and the input frequency 800MHz.

Figure 8: Power Analysis



The Voltage, Current and power can be obtained in the folder after simulation process can be completed.

6.0 Conclusions

In the speech processing the most frequent problem is the consequence of interference noise in speech signals.To tackle this issue,an active noise cancellation architecture based on Zero frequency filter is realized and non voiced classification can be done.The functionality is verified in the Tanner tool with an operating frequency of 800MHz.In this Physical design process delay is achieved through

using the adder circuits.This adders circuit resulted the delay overhead of about approximatly 125ps.

References

[1] R Tsay. Exact zero IS skew clock routing algorithm, Computer Aided Design of Integrated Circuits and Systems,1993, 242-249.

[2] JL Tsai, TH Chen, CC Chen. Zero skew clock-tree optimization with buffer insertion/sizing and wire sizing, Computer Aided design of integrated circuits and systems, 2004, 565-572.

[3] JP Fishburn. Clock skew optimization, IEEE Trans. On computers, 1990, 945-51.

[4] R Deokar, Sapatnekar. A graph-theoretic approach to clock skew optimization, ISCAS, 1994, 407-10.

[5] IS Kourtev, EG Friedman. Clock skew schielding for improved reliability vioa quadratic programming, ICCAD, 1999, 239-43.

[6] V Nawale, TW Chen. Optimal useful cloclk skew scheduling in the presence of variations using robust ILP formmulaions, ICCAD, 2006, 27-32.

[7] V Mehotra, D Boning. Technology scaling impact of variation pn clock skew and interconnect delay, Interconnect Tech, Conference, 2001, 4-6.

[8] K Rajagopal, T Shaked, Y Prasuram, T Cao, A Chowdhury, B Halpin. Timing driven force directed placement with physical net constraints, IPSD, 2003, 60-66.

[9] Y Liu, RS Shelar, J Hui. Delay-optimal simultanwous technology mapping and placement with applications to timing optimization, ICCAD, 2008, 101-106.

[10] SW Hur, A Jagannathan, J Lillis. Timing driven maze routing, TCAD, 2000, 234-241.

[11] K Sato, HEM Kawarabayashi, N Maeda. Post-layout optimization for deep sub-micron design, DAC, 1996, 740-745.

[12] M Ni, SO Memik. A revisit tio the primal-dual basedclock skew scheduling algorithm, ISQED, 2010, 755-764.

[13] J Lu, B Taskin. Post-CTS clock skew scheduling with limited delay buffering, International Midwest Symposium on Circuits and Systems, 2009, 224-227.

[14] W Shen,Y Cai, W Chen, Y Lu, Q Zhou, J Hu. Useful clock skew optimization under a multi-corner mutli-mode design framework, ISQED, 2010, 62-68.

[15] S Roy, PM Mattheakis, LMNavetteand David, Z Pan. Clock Tree Resynthesis for Multi-corner Multi-mode Timing Closure, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 4, 2014.

[16] JM Gorriz, J Ramirez, SCAlvarez, CG Putonet, EW Lang, D Erdogmus. A Novel LMS Algorithm Applied to Adaptive Noise Cancellation, IEEE Signal Processing and Computing Technologies (ICESC), 2014.

[17] MM Dewasthale, RD Khardkar. Acoustic Noise Cancellation Using Adaptive Filters: A Survey, International Conference on Electronic Systems, Signal Processing and Computing Technologies(ICESC), 2014.

[18] KSS Srinivas, Ke Prahallad. An FIR Implementation of Zero Frequency Filtering of Speech Signals, IEEE Trans.Audio, Speech,Lang. Process., 20(9), 2012, 261-2617.

[19] R Smits, B Yegnarayana. Determination of instants of significant excitation in speech using group delay function, IEEe Trans. Speech Audio Process, 3(5), 1995, 325-333.

[20] KS Rao, SRM Prasanna, B Yegnarayana 2007. Determination of instants of Significant Excitation using Hilbert Envelope and Instants of Significant Excitation using Hilbert Envelope and Group Delay Function, IEEE Signal Processing Letters, 14(10), 762-765.

[21] KSR Murty, B Yegnarayana, MA Joseph. Characterization of glotttal activity from speech signals, IEEE Signal Processing Letters, 16(6), 2009, 469-472.

[22] B Yegnarayana, RK Swamy, KSR Murty. Determining mixing parameters from multispeaker data using speech-specific information, IEEE Trans. Audio speech, Lang. Process, 17(6), 2009, 1196-1207.

[23] KSR Murty, B Yegnarayana. Epoch extraction from speech signals, IEEE Trans. Audio, Speech, Lang. Process., 16(8), 2008, 1602-1613.

[24] N Dhanajaya, B Yegnarayana. Voiced /Non Voiced detection based on robustness of voiced ephos, IEEE Signal Processing Letters, 17(3), 2010.

[25] JP Fishburn. Clock skew optimization, IEEE Trans. Computers, 39(7), 1990, 945-951.